IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

an amplifying transistor;

a biasing transistor;

an amplifying side power source line;

a biasing side power source line;

a bias signal line;

an electric discharging transistor; and

an electric discharging power source line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal, ~~and~~

wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor, and

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

2. (Previously presented) A device according to claim 1 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

3. (Previously presented) A device according to claim 1, wherein the electric discharging power source line is connected to the biasing side power source line.

4. (Withdrawn) A device according to claim 1 further comprising at least one selecting switch for controlling an electric current flowing to the output terminal from the amplifying side power source line or from the biasing side power source line.

5. (Canceled)

6. (Withdrawn) A device according to claim 1, wherein a photoelectric conversion element is connected to the input terminal.

7. (Withdrawn) A device according to claim 1, wherein a signal generated by a photoelectric conversion element is fed to the input terminal.

8. (Previously presented) A device according to claim 1, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistors is equivalent to a minimum value of an absolute value of

a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

9. (Previously presented) A device according to claim 1, wherein the amplifying transistor, the biasing transistor, and the electric discharging transistor are transistors having the same polarity.

10. (Previously presented) A scanner, which uses the semiconductor device according to claim 1.

11. (Previously presented) A digital still camera, which uses the semiconductor device according to claim 1.

12. (Previously presented) An X-ray camera, which uses the semiconductor device according to claim 1.

13. (Previously presented) A portable information terminal, which uses the semiconductor device according to claim 1.

14. (Previously presented) A computer, which uses the semiconductor device according to claim 1.

15. (Withdrawn) A device according to claim 2, wherein at least 2 lines from among the

electric discharging power source line, the load capacitance power source line, and the biasing side power source line are connected together.

16. (Withdrawn) A device according to claim 2, wherein the load capacitance power source line is connected to the amplifying side power source line.

17. (Withdrawn) A device according to claim 2 further comprising at least one selecting switch for controlling an electric current flowing to the load capacitance or the output terminal from the amplifying side power source line or from the biasing side power source line.

18. (Withdrawn) A device according to claim 17, wherein the selecting switch has at least one of an N channel transistor or a P channel transistor.

19. (Withdrawn) A device according to claim 6, wherein the photoelectric conversion element is either an X-ray sensor or an infrared sensor.

20. (Withdrawn) A device according to claim 6, wherein the photoelectric conversion element is any one of a photo diode, a Schottky diode, an avalanche diode, or a photo conductor.

21. (Withdrawn) A device according to claim 20, wherein the photo diode is one of a type incorporating a PN type, a PIN type, or an NPN embedded type.

22. (Withdrawn) A device according to claims 6 further comprising a resetting transistor, and

a source terminal or a drain terminal of the resetting transistor is connected to the photoelectric conversion element.

23. (Withdrawn) A semiconductor device comprising: an amplifying transistor;

a biasing transistor;

an amplifying side power source line;

a biasing side power source line;

a signal generating device; and

a bias signal line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal, and wherein the signal generating device is connected to the bias signal line for performing the operation of making the electric potential of the biasing side power source line close to the electric potential of the amplifying side power source line.

24. (Withdrawn) A device according to claim 23 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

25. (Withdrawn) A device according to claim 23 further comprising at least one selecting

switch for controlling an electric current flowing to the output terminal from the amplifying side power source line or from the biasing side power source line.

26. (Withdrawn) A device according to claim 23 wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

27. (Withdrawn) A device according to claim 23, wherein a photoelectric conversion element is connected to the input terminal.

28. (Withdrawn) A device according to claim 23, wherein a signal generated by a photoelectric conversion element is fed to the input terminal.

29. (Withdrawn) A device according to claim 23, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistors is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

30. (Withdrawn) A scanner, which uses the semiconductor device according to claim 23.

31. (Withdrawn) A digital still camera, which uses the semiconductor device according to claim 23.

32. (Withdrawn) An X-ray camera, which uses the semiconductor device according to claim 23.

33. (Withdrawn) A portable information terminal, which uses the semiconductor device according to claim 23.

34. (Withdrawn) A computer, which uses the semiconductor device according to claim 23.

35. (Currently amended) A driving method of a semiconductor device having an amplifying transistor, a biasing transistor, an amplifying side power source line, a biasing side power source line, and a bias signal line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor,

wherein a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal, ~~and~~

wherein the driving method outputs a signal after performing a pre-discharge, and

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

36. (Previously presented) A method according to claim 35 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

37. (Withdrawn) A method according to claim 35, wherein the semiconductor device has at least one selecting switch for controlling an electric current flowing to the output terminal from the amplifying side power source line or from the biasing side power source line.

38. (Canceled)

39. (Withdrawn) A method according to claim 35 further comprising a photoelectric conversion element connected to the input terminal.

40. (Withdrawn) A method according to claim 35, wherein a signal generated by a photoelectric conversion element is fed to the input terminal.

41. (Previously presented) A method according to claim 35, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistor is equivalent to a minimum value of an absolute value of

a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

42. (Withdrawn) A method according to claim 36, wherein at least 2 lines from among the electric discharging power source line, the load capacitance power source line, and the biasing side power source line are to be connected together.

43. (Withdrawn) A method according to claim 36, wherein the load capacitance power source line is connected to the amplifying side power source line.

44. (Withdrawn) A method according claims 36, wherein the semiconductor device has at least one selecting switch for controlling an electric current flowing to the load capacitance or the output terminal from the amplifying side power source line or from the biasing side power source line.

45. (Withdrawn) A method according to claim 44, wherein the selecting switch has at least one of an N channel transistor or a P channel transistor.

46. (Withdrawn) A method according to claim 39, wherein the photoelectric conversion element is either an X-ray sensor or an infrared sensor.

47. (Withdrawn) A method according to claim 39, wherein the photoelectric conversion element is any one of a photo diode, a Schottky diode, an avalanche diode, or a photo conductor.

48. (Withdrawn) A method according to claim 47, wherein the photo diode is any one of a type incorporating a PN type, a PIN type, or an NPN embedded type.

49. (Withdrawn) A method according to claim 39, wherein the semiconductor device has a resetting transistor, and the resetting transistor resets the photoelectric conversion element.

50. (Withdrawn) A driving method of a semiconductor device having an amplifying transistor, a biasing transistor, an amplifying side power source line, a biasing side power source line, and a bias signal line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal, and

wherein the driving method outputs a signal after performing a pre-discharge by making an electric potential of the biasing side power source line close to an electric potential of the amplifying side power source line.

51. (Withdrawn) A method according to claim 50 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

52. (Withdrawn) A method according to claim 50, wherein the semiconductor device has at least one selecting switch for controlling an electric current flowing to the output terminal from the amplifying side power source line or from the biasing side power source line.

53. (Withdrawn) A method according to claim 50, wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

54. (Withdrawn) A method according to claim 50 further comprising a photoelectric conversion element connected to the input terminal.

55. (Withdrawn) A method according to claim 50, wherein a signal generated by a photoelectric conversion element is fed to the input terminal.

56. (Withdrawn) A method according to claim 50, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

57. (Currently amended) A driving method of a semiconductor device having an amplifying

transistor, a biasing transistor, an amplifying side power source line, a biasing side power source line, and a bias signal line, an electric discharging transistor, and an electric discharging power source line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, a source terminal of the amplifying transistor serves as an output terminal, one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor, ~~and~~

wherein the driving method outputs a signal after performing a pre-discharge by making the electric discharging transistor into a conductive state, and

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

58. (Previously presented) A method according to claim 57, wherein a value of an electric potential of the electric discharging power source line takes a value that is between an electric potential of the bias signal line and an electric potential of the biasing side power source line.

59. (Withdrawn) A method according to claim 57 further comprising a load capacitance

wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

60. (Withdrawn) A method according to claim 57, wherein the electric discharging power source line and the biasing side power source line are to be connected together.

61. (Withdrawn) A method according to claim 57, wherein the semiconductor device has at least one selecting switch for controlling an electric current flowing to the output terminal from the amplifying side power source line or from the biasing side power source line.

62. (Canceled)

63. (Withdrawn) A method according to claim 57 further comprising a photoelectric conversion element connected to the input terminal.

64. (Withdrawn) A method according to claim 57, wherein a signal generated by a photoelectric conversion element is fed to the input terminal.

65. (Withdrawn) A method according to claim 57, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

66. (Previously presented) A method according to claims 57, wherein the amplifying transistor, the biasing transistor, and the electric discharging transistor are transistors having the same polarity.

67. (Withdrawn) A driving method of a semiconductor device comprising an electric discharging transistor, an n-channel amplifying transistor and an n-channel biasing transistor, wherein a drain terminal of the n-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the n-channel amplifying transistor is connected to a drain terminal of the n-channel biasing transistor, and a source terminal of the n-channel biasing transistor is connected to a biasing side power source line comprising:

decreasing an electric potential of an output terminal through the electric discharging transistor during a first period, wherein the output terminal is connected to a source terminal of the n-channel amplifying transistor and wherein one of the output terminal and an electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor;

increasing the electric potential of the output terminal through the n-channel amplifying transistor during a second period.

68. (Withdrawn) A driving method of a semiconductor device comprising an n-channel amplifying transistor and an n-channel biasing transistor, wherein a drain terminal of the n-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the n-channel amplifying transistor is connected to a drain terminal of the n-channel biasing transistor,

and a source terminal of the n-channel biasing transistor is connected to a biasing side power source line comprising:

decreasing an electric potential of an output terminal through the n-channel biasing transistor during a first period, wherein the output terminal is connected to a source terminal of the n-channel amplifying transistor;

increasing the electric potential of an output terminal through the n-channel amplifying transistor during a second period;

wherein a gate potential of the n-channel biasing transistor during the first period is lager than a gate potential of the n-channel biasing transistor during the second period.

69. (Withdrawn) A driving method of a semiconductor device comprising an n-channel amplifying transistor, an n-channel biasing transistor, and a bias signal line, wherein a drain terminal of the n-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the n-channel amplifying transistor is connected to a drain terminal of the n-channel biasing transistor, a source terminal of the n-channel biasing transistor is connected to a biasing side power source line, and a gate terminal of the n-channel biasing transistor is connected to the bias signal line comprising:

decreasing an electric potential of an output terminal through the n-channel biasing transistor during a first period, wherein the output terminal is connected to a source terminal of the n-channel amplifying transistor;

increasing the electric potential of an output terminal through the n-channel amplifying transistor during a second period;

wherein a gate potential of the n-channel biasing transistor during the first period is lager than a gate potential of the n-channel biasing transistor during the second period by a signal generating device connected to the bias signal line.

70. (Withdrawn) A driving method of a semiconductor device comprising a p-channel amplifying transistor and a p-channel biasing transistor, wherein a drain terminal of the p-channel amplifying transistor is connected to an amplifying side power source line, a source terminal of the p-channel amplifying transistor is connected to a drain terminal of the p-channel biasing transistor, and a source terminal of the p-channel biasing transistor is connected to a biasing side power source line comprising:

increasing an electric potential of an output terminal through the p-channel biasing transistor during a first period, wherein the output terminal is connected to a source terminal of the p-channel amplifying transistor;

decreasing the electric potential of an output terminal through the p-channel amplifying transistor during a second period;

wherein a gate potential of the p-channel biasing transistor during the first period is lower than a gate potential of the p-channel biasing transistor during the second period.